UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,191	03/11/2004	Ming-Der Lin	MR1035-1424	4737

4586 7590 05/18/2005

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,191	LIN ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-34* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-16, 18-34 in the reply filed on 4/4/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Further, claim 20 comprises the feature "the external carrier substrate is located at the lower surface of the ceramic substrate" *only illustrated in figure 8,* which is related to non-elected species. Therefore, claim 20 is withdrawn from consideration herein.

Claim Objections

Claim 10 is objected to because of the following informalities: --eutectic substrate-- in line 2 of claim 10 should be "eutectic material" to be consistent with claim 11 therein. Appropriate correction is required.

Claim 18 is objected to because of the following informalities: --can be-- in line 2 of claim 18 should be "is". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 26-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 2 and 27, it is not understood how "one or more cavities formed *in* the ceramic substrate" can be obtained since the ceramic substrate 28 in figure 7 of the instant application does not comprise any cavities. However, it appears that "one or more cavities formed *on* the ceramic substrate" can be achieved.

Claim 26 recites the limitation "the conducting layer" in line 5. There is insufficient antecedent basis for this limitation in the claim. The term "conducting layer" was not previously referred to in claim 26.

Claims 3 and 28-34 are also rejected due to their dependency upon the rejected base claims above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-9, 26, 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Sadamasa et al. (US 4,322,735).

Regarding claim 1, Sadamasa et al. discloses on figure 3 a flip chip LED package array comprising a ceramic substrate 33 made of a material capable of

enduring the eutectic temperature of the fabrication process; a metal wire layer 34 (col. 3, line 10) distributed on the surface if the ceramic substrate; and one or more LED chips 37a, 37b (col. 3, line 28) mounted on the metal wire layer on the ceramic substrate, the LED chips being electrically connected together via the metal wire layer to form an electric circuit.

Sadamasa et al. teaches in col. 3, line 9 that the substrate 33 is formed of alumina (Al_2O_3), and applicant teaches in page 5, lines 5-8 of the instant application the ceramic substrate which is made of Al_2O_3 is capable of enduring the eutectic temperature of the fabrication process. Therefore, the ceramic substrate of Sadamasa et al. meets the claim.

Regarding claim 7, Sadamasa et al. discloses that the material of the ceramic substrate is selected from Al_2O_3 (col. 3, line 9). Note that Al_2O_3 is also known as alumina.

Regarding claim 8, Sadamasa et al. discloses on figure 4 the electric circuit is in one of the forms consisting of parallel (col. 5, line 2). Note that LED 55a and LED 55b are in parallel with each other.

Regarding claim 9, Sadamasa et al. discloses on figure 3 a metal plate 32 (col. 3, lines 3-4) is further disposed on another surface of the ceramic substrate 33.

Regarding claim 26, as best understood, Sadamasa et al. discloses on figure 3 a flip chip LED package comprising a ceramic substrate 33 (col. 3, line 9) made of a material capable of enduring the eutectic temperature of the fabrication process; a metal wire layer 34 (col. 3, line 10) distributed on the surface of the ceramic substrate; at least

an LED chip 37a (col. 3, line 28) mounted on the conducting layer on the ceramic substrate to achieve electric connection.

Regarding claim 31, Sadamasa et al. discloses that the material of the ceramic substrate is selected from Al_2O_3 (col. 3, line 9).

Regarding claim 32, Sadamasa et al. discloses on figure 3 a metal plate 32 (col. 3, lines 3-4) is further disposed on another surface of the ceramic substrate 33.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al. and further in view of Hayashimoto et al. (US 2004/0211970 A1).

Regarding claims 2 and 27, as best understood, Sadamasa et al. teaches about the *ceramic* substrate 33 (col. 3, line 9). Sadamasa et al. does not teach one cavity formed in the substrate to accommodate the LED chip. However, Hayashimoto et al. discloses on figure 1 one cavity 18 formed in the substrate to accommodate the LED chip. Note that element 18 forms one cavity in the substrate. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al. by having one cavity formed in the substrate to accommodate the LED chip for the purpose of improving the light output efficiency.

Regarding claims 3 and 28, as best understood, Hayashimoto et al. discloses on figure 1 a reflecting film 19 (para [0045], lines 2-3) is formed on the surface of each of the cavities 18. Note that even though element 19 is an insulation film, it can function as a reflecting film as shown in figure 1 where light is reflected from element 19.

Regarding claims 4 and 29, Hayashimoto et al. discloses on figure 1 a reflecting cover 18 (para [0045], line 1) is annularly formed around each of the LED chips.

Note that element 18 has a similar structure as that of reflecting cover 46 in figure 7 of the instant application. Therefore, element 18 is considered "reflecting cover". Further, it is clear that the reflecting cover 18 is annularly formed around each of the LED chips as seen from the top view.

Regarding claim 5, Hayashimoto et al. discloses on figure 1 the reflecting cover 18 has one LED chip 11 (para [0034], line 5).

Claims 6 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al. and Hayashimoto et al. and further in view of Oshio et al. (US 6,274,890)

Regarding claims 6 and 30, Sadamasa et al. and Hayashimoto et al. disclose substantially all the structure set forth in the claimed invention except a lens covering the upper surface of the reflecting cover. However, Oshio et al. discloses on figure 1 a lens 9 (col.6, line 1) covering the upper surface of the reflecting cover 10a. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al. and Hayashimoto et al. by having a

lens covering the upper surface of the reflecting cover for the purpose of improving the light take out efficiency (col. 1, lines 63-64 of Oshio et al.).

Claims 10, 11, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al. and further in view of Kim (US 2005/0077532A1).

Regarding claims 10 and 33, Sadamasa et al. discloses on figure 3 substantially all the structure set forth in the claimed invention except the LEDs mounted on the metal wire layer by using a eutectic substrate. However, Kim shows in figure 3c the LEDs 170 (para [0043], line 2) mounted on the metal wire layer 164 (para [0042], line 7) by using a eutectic substrate 168 (para [0042], lines 20-22). Note that Kim teaches in para [0042], lines 20-22 that element 168 is formed of Au-Sn which is the same eutectic material being used in the instant application (page 5, line 9). Therefore, the eutectic substrate of Kim meets the claim. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al. by having the LEDs mounted on the metal wire layer by using a eutectic substrate for the purpose of further strengthening the bonding between the LED chips and the metal wire therein.

Regarding claims 11 and 34, Kim teaches that the eutectic material is Au-Sn (para [0042], line 7).

Claims 12-13, 16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al in view of Oshio et al.

Regarding claim 12, Sadamasa et al. discloses on figure 3 a flip chip LED package unit comprising a metal body 32 (col. 3, line 1); a ceramic substrate 33 mounted on the metal body, a conducting layer 34 (col. 3, line 10) on the ceramic substrate to achieve electric connection, the ceramic substrate being made of a material having an coefficiency of thermal expansion matched with the LED chips 37a, 37b; an external carrier substrate 47 arranged on the metal body 32, the LED chip achieving electric connection with the external via the conducting layer 34 as external conducting contacts, wherein the external carrier substrate is a metal lead frame (col. 4, line 3).

Sadamasa et al. teaches in col. 3, line 9 that the substrate 33 is formed of alumina (Al_2O_3), and applicant teaches in page 5, lines 6-8 of the instant application the ceramic substrate which is made of Al_2O_3 is having an coefficiency of thermal expansion matched with the LED chips. Therefore, the ceramic substrate of Sadamasa et al. meets the claim.

Sadamasa et al. does not teach a lens covering the LED chip. However, Oshio et al. discloses on figure 1 a lens 9 (col. 6, line 1) covering the LED chip 1. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al. by having a lens covering the LED chip for the purpose of improving the light take out efficiency (col. 1, lines 63-64 of Oshio et al.).

Regarding claim 13, Oshio et al. disclose on figure 1 a reflecting cover 10a (col. 5, line 45) annularly disposed on the external carrier substrate 22 (col. 6, line 18) around the LED chip 1 so that the lens 9 can be mounted on the reflecting cover 10a.

Note that the reflecting cover 10a is annularly formed around the LED chip 1 as seen from the top view.

Regarding claim 16, Sadamasa et al. discloses that the material of the ceramic substrate is selected from Al_2O_3 (col. 3, line 9).

Regarding claim 18, the claim language is merely product by process and therefore does not structurally distinguish from Sadamasa et al. and Oshio et al. herein.

Regarding claim 19, Sadamasa et al. discloses on figure 3 the conducting layer 34 on the ceramic substrate 33 achieves electric connection with the external carrier substrate 47 by using one or more metal wire 39 (col. 3, line 59).

Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al and Oshio et al., and further in view of Hayashimoto et al.

Regarding claim 14, Sadamasa et al and Oshio et al. together disclose substantially all the structure set forth in the claimed invention except a reflecting film formed on the inner surface of the reflecting cover. However, Hayashimoto et al. discloses on figure 1 a reflecting film 19 formed on the inner surface of the reflecting cover 18. Note that even though element 19 is an insulation film, it can function as a reflecting film as shown in figure 1 where light is reflected from element 19.

In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al and Oshio et al. by having a reflecting film formed on the inner surface of the reflecting cover for the purpose of increasing the light output efficiency.

Regarding claim 15, Hayashimoto et al. discloses on figure 1 the reflecting cover 18 is mounted on the external carrier substrate 12 by using a non-conducting attach 19. Note that the bottom surface of the reflecting cover 18 is covered with insulation film 19 and therefore the reflecting cover 18 is mounted on the external carrier substrate via a non conducting attach 19.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al. and Oshio et al., and further in view of Newby (US 2005/0024834 A1).

Regarding claim 21, Sadamasa et al. discloses on figure 3 the ceramic substrate 33. Sadamasa et al. Oshio et al. do not teach a metal heat-radiating fin disposed on the lower surface of the substrate. However, Newby teaches on figure 5B a metal heat radiating fin 46 (para [0015], line 3) disposed on the lower surface of the substrate 22 (para [0003], line 3). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al. and Oshio et al. by having a metal heat-radiating fin disposed on the lower surface of the substrate for the purpose of effectively dissipating heat away from the LED chip.

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al. and Oshio et al., and further in view of Kim (US 2005/0077532A1).

Regarding claims 22, Sadamasa et al and Oshio et al. discloses substantially all the structure set forth in the claimed invention except the LED chip mounted on the

metal wire layer by using a eutectic material. However, Kim teaches on figure 3c the LED chip 170 (para [0043], line 3) mounted on the metal wire layer 164 (para [0042], line 7) by using a eutectic material 168 (para [0042], lines 20-22). Note that Kim teaches in para [0042], line 7 that element 168 is formed of Au-Sn, which is the same eutectic material being used in the instant application (page 5, line 9). Therefore, Kim teaches about the eutectic material. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al. and Oshio et al. by having the LEDs mounted on the metal wire layer by using a eutectic substrate for the purpose of further strengthening the bonding between the LED chips and the meta wire therein.

Regarding claim 23, Kim teaches that the eutectic material is Au-Sn (para [0042], line 7).

Claim 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sadamasa et al and Oshio et al., and further in view of Harrah et al. (US 6,498,355 B1)

Regarding claim 24, Sadamasa et al. discloses on figure 3 the ceramic substrate on the metal body 32. Sadamasa et al. and Oshio et al. do not disclose the ceramic substrate mounted on the metal body by a thermal conductive adhesive. However, Harrah et al. discloses on figure 3 the ceramic substrate 30 (col. 4, lines 38-40) mounted on the metal body 6 (col. 2, line 51) by a thermal conductive adhesive 24 (col. 3, lines 48-49). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sadamasa et al and Oshio

et al. by having the ceramic substrate mounted on the metal body by a thermal conductive adhesive for the purpose of further strengthening the bonding between the substrate and the metal body.

Regarding claim 25, Harrah et al. teaches that the material of the metal body 6 includes copper (col. 3, line 54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
May 16, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER